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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,770	TANI ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Also, acknowledged the receipt of the priority documents, which have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bovensiepen et al., (US Patent No. 6,222,740), in view of Echigo et al., (US Patent No. 6,274,821).

Regarding claim 1, Bovensiepen et al., in an alternate embodiment of figure 1, discloses a multilayer wiring board comprising: a core portion (5) including a core insulating layer (core layer 30) containing a carbon fiber material (carbon fiber core, column 5, line 35-36); a first lamination wiring portion (12,22) bonded to the core portion and having a laminated structure including at least a first insulating layer (22) and a first wiring pattern (12); and a second lamination wiring portion (11,21) bonded to the first

lamination wiring portion and having a laminated structure including at least a second insulating layer (21)and a second wiring pattern (11); wherein the core portion, the first lamination wiring portion and the second lamination wiring portion are arranged in a stack (all the layers are stacked, see figure 1).

Bovensiepen et al., does not disclose the first insulating layer containing glass cloth. Bovensiepen et al., discloses the insulating layers made of glass epoxy, (column 3,line 54-55).

Echigo et al., discloses a printed circuit board and further recites "[C]onventionally, a printed circuit board for mounting electronic parts is composed of a glass-epoxy substrate including laminated sheets, each of which is made of a glass cloth impregnated with epoxy-pregreg. This kind of circuit board has been generally used with high reliability for mounting parts".

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the circuit board of Bovensiepen et al., with the first insulating layer containing glass cloth, at taught by Echigo et al., in order to have high reliability substrate.

Regarding claim 2, Bovensiepen et al., in an alternate embodiment of figure 1, discloses a multilayer wiring board comprising: a core portion including a core insulating

layer (core layer 30) containing a carbon fiber material (carbon fiber core, column 5, line 35-36); two first lamination wiring portions (12,22 and 13,23) respectively bonded to opposite sides of the core portion, each of the first lamination wiring portions having a laminated structure including at least a first insulating layer (22,23) and a first wiring pattern (12,13); and a second lamination wiring portion (11,21) bonded to one of the first lamination wiring portions and having a laminated structure including at least a second insulating layer (21) and a second wiring pattern (11); wherein the core portion, the first lamination wiring portions and the second lamination wiring portion are arranged in a stack (all the layers are stacked, see figure 1).

Bovensiepen et al., does not disclose the first insulating layer containing glass cloth. Bovensiepen et al., discloses the insulating layers made of glass epoxy, (column 3,line 54-55).

Echigo et al., discloses a printed circuit board and further recites "[C]onventionally, a printed circuit board for mounting electronic parts is composed of a glass-epoxy substrate including laminated sheets, each of which is made of a glass cloth impregnated with epoxy-pregreg. This kind of circuit board has been generally used with high reliability for mounting parts".

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the circuit board of Bovensiepen et al., with

the first insulating layer containing glass cloth, at taught by Echigo et al., in order to have high reliability substrate.

Regarding claim 3, Bovensiepen et al., further discloses an additional second lamination wiring portion (14,24), wherein the additional second lamination wiring portion has a laminated structure including at least a second insulating layer (24) and a second wiring pattern (14), and is bonded to the first lamination wiring portion other than said one of the first lamination wiring portions (bonded to laminate 13,23, see figure 1).

Regarding claim 6, Bovensiepen et al., further discloses the carbon fiber material is provided in a form of nonwoven fabric (carbon fiber piles, column 5, line 38-45).

Regarding claim 9, Bovensiepen et al., further discloses the core insulating layer is formed of a material containing epoxy resin (column 5,line 42).

4. Claims 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the modified circuit board Bovensiepen et al., (in combination with Echigo et al.), as applied to claim 1 above, and further in view of Vasoya et al., (US Patent Publication No. 2002/0157859), Yuhas et al., (US Patent No. 5,350,621) and Hoebener et al., (US Patent No. 5,825,629).

Regarding claim 7, Bovensiepen et al., discloses all the features of the claimed invention, as applied to claim 1 above, but does not disclose the core insulating layer contains the carbon fiber material at a rate of 30 through 80 vol %. However, the core layer, layer with carbon fiber, is used for reducing the overall coefficient of thermal expansion of the circuit board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device (column 1, line 1-30)

Vasoya et al. discloses a circuit board and recites that Carbon fibers have low coefficient of thermal expansion, in the range of –0.3 to 3.0 ppm / K, (column 2, paragraph [0026].

Hoebener et al., discloses a circuit board and recites that FR4 board material exhibit a nominal coefficient of thermal expansion between 15-20 ppm/K and BT resin board has the coefficient of thermal expansion in the range of 10-20 ppm/K, column 6, line 23-45.

Yuhas et al., discloses electronic laminates and recites that coefficient of thermal expansion epoxy resin is between 55 to 65 ppm/k.

A person of ordinary skill in the art would adjust the proportion of the carbon content in the core layer to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art, *In re Boesch*, 617 F.2d 272, 205 US PQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at time of applicant's invention to further modify wiring board of Bovensiepen et al., with the core insulating layer contains the carbon fiber material at a rate of 30 through 80 vol %, from the teachings of Vasoya et al., Hoebener et al., and Yuhas et al., in order to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Regarding claim 8, Bovensiepen et al., discloses all the features of the claimed invention, as applied to claim 1 above, but does not disclose the carbon fiber material is graphitized at a rate not smaller than 99%. However, the core layer, layer with carbon fiber, is used for reducing the overall coefficient of thermal expansion of the circuit board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device (column 1, line 1-30)

Vasoya et al. discloses a circuit board and recites that Carbon fibers have low coefficient of thermal expansion, in the range of –0.3 to 3.0 ppm / K, (column 2, paragraph [0026].

Hoebener et al., discloses a circuit board and recites that FR4 board material exhibit a nominal coefficient of thermal expansion between 15-20 ppm/K and BT resin board has the coefficient of thermal expansion in the range of 10-20 ppm/K, column 6, line 23-45.

Yuhas et al., discloses electronic laminates and recites that coefficient of thermal expansion epoxy resin is between 55 to 65 ppm/k.

A person of ordinary skill in the art would adjust the proportion of the carbon (graphite) content in the core layer to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art, *In re Boesch*, 617 F.2d 272, 205 US PQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at time of applicant's invention to further modify wiring board of Bovensiepen et al., the carbon fiber material is graphitized at a rate not smaller than 99%, from the teachings of Vasoya et al., Hoebener et al., and Yuhas et al., in order to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Regarding claim 5, Bovensiepen et al., discloses all the features of the claimed invention, as applied to claim 1 above, but does not disclose the core insulating layer, the first insulating layer and the second insulating layer have respective thermal expansion coefficients defined in a surface-spreading direction transverse to a stacking direction of these three layers, the thermal expansion coefficient of the core insulating layer being no smaller than -3 ppm/K but smaller than 8 ppm/K below 150.degree. C., the thermal expansion coefficient of the first insulating layer being no smaller than 8 ppm/K but smaller than 20 ppm/K below 150.degree. C., the thermal expansion coefficient of the second insulating layer being no smaller than 20 ppm/K but smaller than 100 ppm/K below 150.degree. C.

However, Bovensiepen et al., further recites that high thermal coefficient of the circuit board material (approx. 15 ppm/k) is reduced by relatively low coefficient of thermal expansion of the core (approx. 5.3 ppm/k, with molybdenum as core material in one embodiment and core with carbon fiber in the other embodiment, (column 4, line 50-65 and column 5, line 34-50). Furthermore, the core layer, layer with carbon fiber, of Bovensiepen et al., is used for reducing the overall coefficient of thermal expansion of the circuit board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device (column 1, line 1-30)

Vasoya et al. discloses a circuit board and recites that Carbon fibers have low coefficient of thermal expansion, in the range of –0.3 to 3.0 ppm / K, (column 2, paragraph [0026].

Hoebener et al., discloses a circuit board and recites that FR4 board material exhibit a nominal coefficient of thermal expansion between 15-20 ppm/K and BT resin board has the coefficient of thermal expansion in the range of 10-20 ppm/K, column 6, line 23-45.

Yuhas et al., discloses electronic laminates and recites that coefficient of thermal expansion epoxy resin is between 55 to 65 ppm/k.

A person of ordinary skill in the art would adjust the proportion of the coefficient of thermal expansion of insulating layer and the core layer to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art, *In re Boesch*, 617 F.2d 272, 205 US PQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at time of applicant's invention to further modify wiring board of Bovensiepen et al., the core insulating layer, the first insulating layer and the second insulating layer have respective thermal expansion coefficients defined in a surface-spreading direction transverse to a stacking direction of these three layers, the thermal expansion coefficient of the core insulating layer being no smaller than -3 ppm/K but smaller than 8 ppm/K below 150.degree. C., the thermal expansion coefficient of the first insulating layer being no smaller than 8 ppm/K but smaller than 20 ppm/K below 150.degree. C.,

the thermal expansion coefficient of the second insulating layer being no smaller than 20 ppm/K but smaller than 100 ppm/K below 150.degree. C, from the teachings of Vasoya et al., Hoebener et al., and Yuhas et al., in order to reduce the over all coefficient of thermal expansion of the board to adapt to that of the component to reduce the shear forces at the connection of the component to the board to avoid damage and improve the performance of the device.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-4, 6, 7 and 9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 6, 7 and 12 of U.S. Patent No. 6,869,665, hereafter pat665, in view of Echigo et al., (US Patent No. 6,274,821) and Alcoe et al., US Patent Publication No. 2002/0139578.

Regarding claim 1, claim 1 of Pat665 discloses a multilayer wiring board comprising: a core portion (core portion of the core layer without the via hole and

insulating resin around via hole, claim 1, line 13-16) including a core insulating layer (core layer, claim 1, line 2) containing a carbon fiber material (carbon fiber, claim 1, line 2); a first lamination wiring portion bonded to the core portion and having a laminated structure including at least a first insulating layer and a first wiring pattern (claim 1, line 6-8).

Claim 1 of Pat665 does not disclose the first insulating layer containing glass cloth; and a second lamination wiring portion bonded to the first lamination wiring portion and having a laminated structure including at least a second insulating layer and a second wiring pattern; wherein the core portion, the first lamination wiring portion and the second lamination wiring portion are arranged in a stack.

Echigo et al., discloses a printed circuit board and further recites "[C]onventionally, a printed circuit board for mounting electronic parts is composed of a glass-epoxy substrate including laminated sheets, each of which is made of a glass cloth impregnated with epoxy-pregreg. This kind of circuit board has been generally used with high reliability for mounting parts.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the circuit board of Claim 1 of Pat665 with the first insulating layer containing glass cloth, at taught by Echigo et al., in order to have high reliability substrate.

Alcoe et al., in figure 2, discloses an electronic structure with multiple laminates on the core substrate to increase overall wiring density (page 4, paragraph 0039).

A person of ordinary skill in the art at the time of applicant's invention would have found advantages to provide a second laminating layer bonded to the first lamination wiring portion to increase the wiring density of the electronic structure.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the circuit board of Pat665 with a second lamination wiring portion bonded to the first lamination wiring portion and having a laminated structure including at least a second insulating layer and a second wiring pattern; wherein the core portion, the first lamination wiring portion and the second lamination wiring portion are arranged in a stack, as taught by Alcoe et al., in order to increase the wiring density of the circuit board.

Regarding claim 2, Claim 1 of Pat665 discloses multilayer wiring board comprising: a core portion (core portion of the core layer without the via hole and insulating resin around via hole, claim 1, line 13-16) including a core insulating layer (core layer, claim 1, line 2) containing a carbon fiber material (carbon fiber, claim 1, line 2); two first lamination wiring portions respectively bonded to opposite sides of the core portion (claim 1, line 6-8 and claim 2, line 1-4), each of the first lamination wiring portions having a laminated structure including at least a first insulating layer and a first wiring pattern.

Claim 1 of Pat665 does not disclose the first insulating layer containing glass cloth; and a second lamination wiring portion bonded to the first lamination wiring portion and having a laminated structure including at least a second insulating layer and a second wiring pattern; wherein the core portion, the first lamination wiring portion and the second lamination wiring portion are arranged in a stack.

Echigo et al., discloses a printed circuit board and further recites that "[C]onventionally, a printed circuit board for mounting electronic parts is composed of a glass-epoxy substrate including laminated sheets, each of which is made of a glass cloth impregnated with epoxy-pregreg. This kind of circuit board has been generally used with high reliability for mounting parts.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the circuit board of claim 1 of Pat665 with the first insulating layer containing glass cloth, at taught by Echigo et al., in order to have high reliability substrate.

Alcoe et al., in figure 2, discloses an electronic structure with multiple laminates on the core substrate to increase overall wiring density (page 4, paragraph 0039).

A person of ordinary skill in the art at the time of applicant's invention would have found advantages to provide as second laminating layer bonded to the first lamination wiring portion to increase the wiring density of the electronic structure.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the circuit board of claim 1 of Pat665 with a second lamination wiring portion bonded to the first lamination wiring portion and having a laminated structure including at least a second insulating layer and a second wiring pattern; wherein the core portion, the first lamination wiring portion and the second lamination wiring portion are arranged in a stack, as taught by Alcoe et al., in order to increase the wiring density of the circuit board.

Regarding claim 3, the modified claim 1 of Pat665 discloses all the features of the claimed invention as applied to claim 2 above, but fails to disclose an additional second lamination wiring portion, wherein the additional second lamination wiring portion has a laminated structure including at least a second insulating layer and a second wiring pattern, and is bonded to the first lamination wiring portion other than said one of the first lamination wiring portions.

Alcoe et al., in figure 2, discloses an electronic structure with multiple laminates on the other side of the core substrate to increase overall wiring density (page 4, paragraph 0039).

A person of ordinary skill in the art at the time of applicant's invention would have found advantages to provide as second laminating layer bonded to the other of the first lamination wiring portion to increase the wiring density of the electronic structure.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the circuit board of Pat665 with an

additional second lamination wiring portion, wherein the additional second lamination wiring portion has a laminated structure including at least a second insulating layer and a second wiring pattern, and is bonded to the first lamination wiring portion other than said one of the first lamination wiring portions, as taught by Alcoe et al., in order to increase the wiring density of the circuit board.

Regarding claim 4, Pat665 discloses all the features of the claimed invention as applied to claim 1 above, including the through hole via insulated from the core portion by an insulating layer core portion by an insulating layer surrounding the through-hole via (line 9-17, claim 1). However, does not disclose the through via extending through both the core portion and the first lamination wiring portion. Claim 1 of Pat 665 discloses via passing through the core substrate and electrically connected to the first wiring pattern.

Alcoe et al., in figure 2, discloses an electronic structure with via (30, 31,32) penetrating the core substrate (20) and laminating substrates (laminates above and below the core substrate 20) to facilitate connection of the via to outside terminals.

Therefore, it would have been obvious to a person of ordinary skill in the art to further modify the circuit board of Pat665 to have the through via extending through both the core portion and the first lamination wiring portion, as taught by Alcoe et al., in order to facilitate connection of the via to outside terminals.

Regarding claim 6, the modified board of Pat665 discloses all the features of the claimed invention as applied to claim 1 above including the carbon fiber material is provided in a form of mesh, cloth or nonwoven fabric (Pat665, claim 6).

Regarding claim 7, the modified board of Pat665 discloses all the features of the claimed invention as applied to claim 1, including the core insulating layer contains the carbon fiber material at a rate of 30 through 80 vol % (Pat665, claim 7).

Regarding claim 9, the modified board of Pat665 discloses all the features of the claimed invention as applied to claim 1, including the core insulating layer is formed of a material containing a resin that is selected from a group consisting of: polysulfone, polyethersulfone, polyphenylsulfone, polyphthalamide, polyamideimide, polyketone, polyacetal, polyimide, polycarbonate, modified-polyphenyleneether, polyphenyleneoxide, polybutyreneterephthalate, polyacrylate, polyphenylenesulfide, polyetheretherketone, tetrafluoroethylene, epoxy, cyanateester, and bismaleimide (Pat665, claim 12).

Conclusion

7. No prior art rejection is given to claim 4 except the double patenting rejection.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Japp et al. US Patent No. 6,613,413, discloses a multilayer circuit board with power / ground core made of carbon fiber coated with metal to increase the conductivity of base material, column 6, line 33-45).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IB Patel

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
April 26, 2005